Department of Computer Science & Engg.
CSL 211 Computer Architecture : Major Test

Date: 30.11.2006 Time: 13:00-15:00 Max marks: 30

1. A pipelined processor does target address calculation for branch instructions in i^{th} cycle and takes the decision to branch in j^{th} cycle ($i < j$). The next instruction after branch (*inline* or *target*) is fetched in cycle $j+1$. Find the average number of cycles lost per instruction due to control hazards if 20% of all the instructions are branch instructions. Recalculate this figure assuming static branch prediction in k^{th} cycle ($k < i$), such that 60% of *taken branches* and 80% of *not taken branches* are correctly predicted. How would this figure change if dynamic branch prediction is used in place of static branch prediction, resulting in improving the prediction accuracy of the taken branches to 80% and also making the target address available in k^{th} cycle.

(8)

2. Draw a flow chart showing how memory access will be done, beginning with a virtual address, in a system with TLB and physically addressed cache. Assume that the page table is in the physical memory and parts of it could be in the cache. Using the following data, find average memory access time.

TLB	access time = 1 cycle; miss rate = 4%
Cache	access time = 1 cycle; miss rate = 1%; WB policy; dirty blocks = 20%
Physical memory	block transfer time = 20 cycles
Virtual memory	page fault = .001%; page fault service time = 10^6 cycles page table entry address calculation = 1 cycle

(7)

3. Consider a processor with the following MIPS instruction subset -{add, sub, and, or, lw, sw, beq, j}. It directly accesses the physical memory for the program but uses virtual memory for data. The page table is stored in the physical memory, with its starting address contained in a special register. Assume that there is neither a cache nor a TLB and access to the physical memory is made in a single cycle. Further, the data path has a single ALU for doing all additions/subtractions. The following exceptions are defined for this processor : overflow, illegal opcode and page fault. Design a controller for this processor using multi-cycle approach. You only need to show the state diagram/flow chart along with the associated actions.

(7)

4. A web server needs to be designed as per the architecture shown below to service 500 requests per second on average. Each request is received in the form of a 256 byte packet. Only 1% of the requests are for a file download (average size 1MB), 5% are for web pages with graphics (average size 200KB) and the remaining 94% are for textual web pages (average size 10KB). All the data is sent over the network in the form of 1 KB packets. Each packet has 100 bytes of header information in addition to 256B / 1KB of data. Each disk drive has a data transfer rate of 5 MB/s, a rotational speed of 10,000 rpm and an average seek time of 5 ms. The disk read operations are in terms of 10 KB at a time. The web server process executes 10,000 instructions per request. Apart from this, the operating system requires 10,000 instructions per disk read and 2,000 instructions per packet input/output (including processing/creation of packet header). Because of cache misses, transfer of one cache block of size 64 bytes is required per 100 instructions between memory and cache. Give CPU MIPS, P-M bus bandwidth, I/O bus bandwidth, number of disk drives and network bandwidth to meet these requirements?

(8)