Major EEL 201 Digital Electronic Circuits

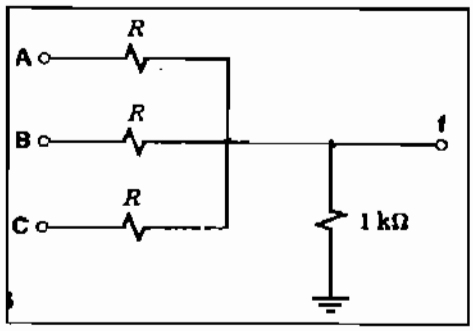
Time: 2 Hour **1/12/06** **Max. Marks: 55**

Name:	Entry #	Group #

N.B.: Attempt all questions. Answer at the appropriate locations as indicated. For all calculations and rough work use the *reverse side / extra sheets* provided.

Q1a. The '**resistor logic**' circuit has binary inputs (A, B, C), of '**0**' V and '**4**' V (for '**low**' and '**high**' levels).

For **R = 2 KΩ**, compute and fill the truth-table showing *actual voltages* for 'f' by filling in the given table on the right.

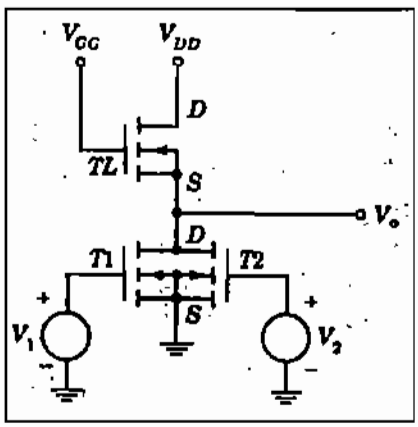


A	B	C	f volt
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Q1b. In the given NMOS transistors based logic circuit, **T1** and **T2** are placed in parallel. Supply voltages V_{DD} and V_{GG} are positive (set to Logic **HIGH** or **1**). Write the truth-table for V_0 as a function of V_1 and V_2.

(4 + 4 = 8 marks)

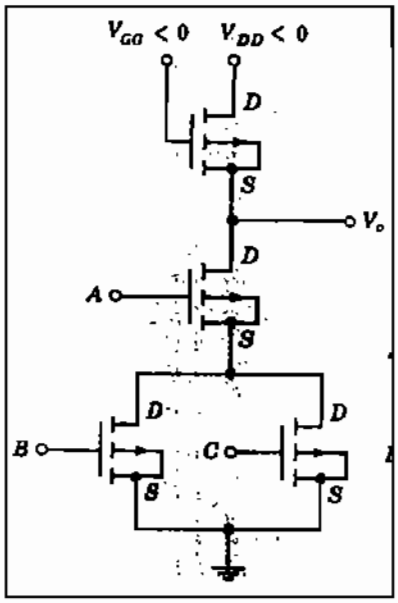
V_1	V_2	V_0



PTO

Q2a. In the given PMOS transistor based logic circuit, output V_0 is a function of three inputs A, B and C.
A (OR, AND) logic gate circuit is also shown, but without proper inputs marked.
For the two circuits to be equivalent, write the three inputs in the appropriate form, on the gate circuit.

(3 marks)

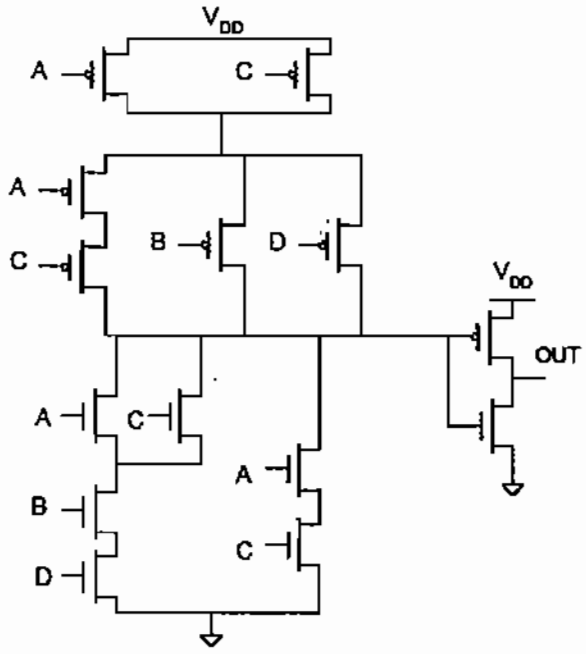


Q2b. For the given **CMOS** circuit, write the output (**OUT**) as a function of the inputs (**A, B, C, D**) in **SOP** form.

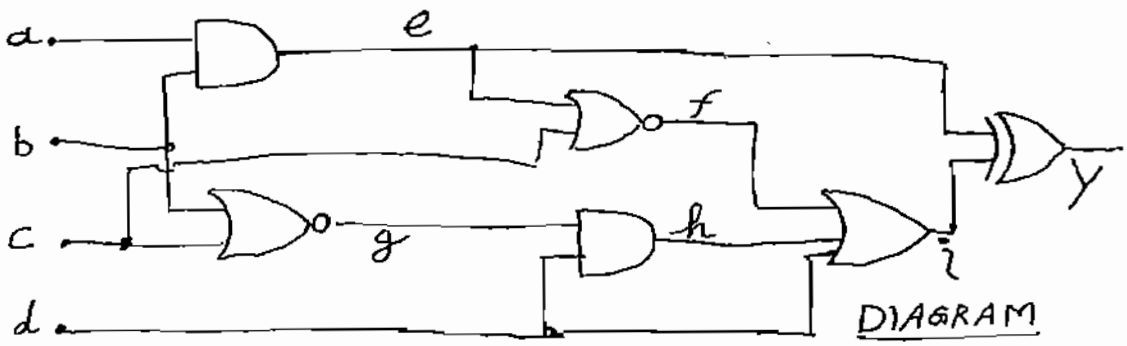
(5 marks)

Answer:

OUT =



Q3:- Using **diagram given below** compute '**Y**' as a function of input signals. Using Boolean Difference method fid out which of the **faults** at '**h**' can not be tested? (Answer within **20** words to justify your **logic/proof** after derivations) Then compute all tests for the fault '**f**'**s-a-0** by means of Boolean Difference method. **(8)**



DIAGRAM

Calculations: **Y =**

Answer: The fault/faults which can not be tested at '**h**' is/are = ...
The reason is…

The tests for '**f's-a-0** are as given below:

a	**b**	**c**	**d**
↓	↓	↓	↓

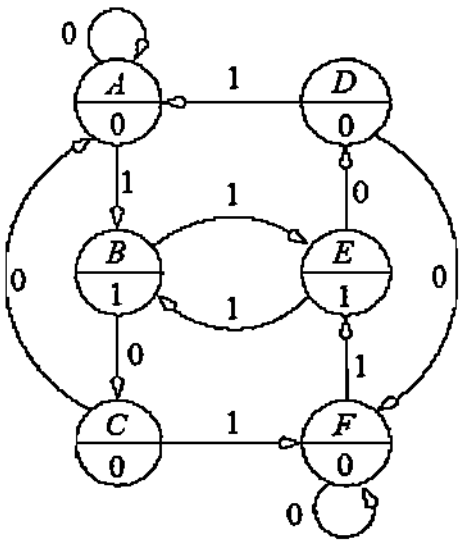
1st ----------

2nd ----------

3rd ----------

4th ----------

Q4 (a):- Minimize the finite state machine given below using implication chart method.

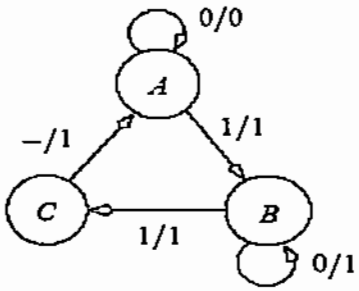


B					
C					
D					
E					
F					
	A	**B**	**C**	**D**	**E**

Answer: The equivalent states are as ---

The minimized finite state machine is as:

(b):- Convert the given **Mealy** machine into **Moore** machine.



ANSWER:- Draw equivalent machine below:

(6 + 3)

Q 5 (a):- Initial value of **CY** flag is **0.** Write the value of **CY** flag and accumulator after the execution of instructions labled as 1, 2, 3, 4, 5 and 6. Assume the value of **mn H = 59 H**

```
        MVI  A, mn H
        RAL
(1)     ADI  E1 H
        MVI  B, 04 H
        ANI  FF H
(2)     ADC  B
        XRI  mn H
        MVI  C, 01 H
(3)     RRC
        MVI  B, 10 H
(4)     ORA  B
        LXI  H, 1234 H
        LXI  B,  5678 H
        LXI  D,  2468 H
        ADD  C
(5)     DAA
(6)     DAD  B
```

Answers: List the answers as indicated

	CY	$A = B_7$	B_6	B_5	B_4	B_3	B_2	B_1	B_0
	↓	↓		↓	↓	↓	↓	↓	↓
1st									
2nd									
3rd									
4th									
5th									
6th									

(b) Find and write **only** accumulator values after the execution of instructions labled as 1 and 2. **(6+3)**

```
        LXI  B, 3386 H
        LXI  D, 9533 H
        MVI  A, 57 H
(1)     ADD  C
        DAA
        CMP  E
        SUB  D
(2)     STC
```

Answer:

	$A = B_7$	B_6	B_5	B_4	B_3	B_2	B_1	B_0
	↓	↓	↓	↓	↓	↓	↓	↓
1st								
2nd								

Q6:- For the circuit given in figure (3) below answer the questios as indicated. **(6)**

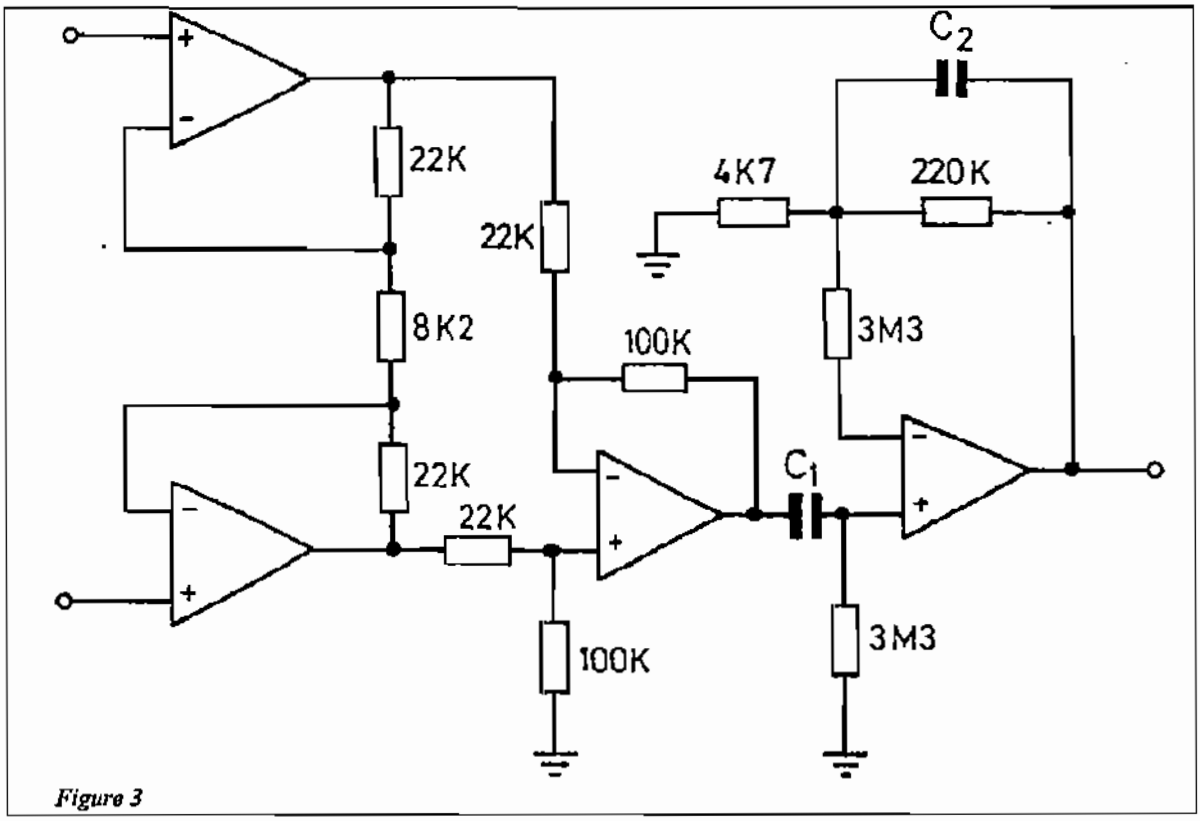


Figure 3

Here 3M3 implies 3.3 M. Ohm and similarly others.

(a) - What is the d.c. gain of the input stages (excluding the rightmost opamp)?

Answer:

(b) - If C_1 = 1 microfard what is the lower cutoff frequency?

Answer:

(c) - If C_2 = 0.0033 microfard what is the upper cutoff frequency?

Answer:

(d) - What is the overall gain of the circuit at the mid–band frequency?

Answer:

Q7:- Data appearing on a line synchronized with a clock should never have three or more consecutive **0**'s or four or more consecutive **1**'s.
Design a sequential circuit that will detect such sequences and generate an output of **1** whenever they occur. Construct appropriate timing diagrams for different combination of inputs. **(7)**

Answer:-