INDIAN INSTITUTE OF TECHNOLOGY DELHI

EEL 201 Digital Electronic Circuits

Minor 1

Date: September 2, 2013 Time: 7:00 – 8:00PM

1. Two decimal numbers, both between 0 and 9, need to be added to each other. Design a logic circuit that performs a BCD addition of these two numbers. Use block diagrams for adders and other components that you need, use any combinational logic gates that you require. (3)

2. (a) A 7 bit number is 1101011. What does it represent if the binary number was (i) in sign-magnitude notation (ii) in 2's complement notation (iii) in offset binary notation?
(b) Convert the decimal number 49.3 to octal representation. (3+1)

3. When making a normal encoder circuit it converts base 4 input, represented by four lines each representing a number in base 4 number, to binary output represented by 2 lines. In a normal base 4 number to binary encoder, only one of the four inputs will be 1, the input being labeled I_3, I_2, I_1 and I_0. For example if I_3 is 1 and the rest 0 the encoded output, represented by lines Z_1 Z_0, will be 11. In a priority encoder more than one of the inputs could have a value 1, unlike in a normal base 4 number to binary encoder. We need to design a priority encoder that encodes such that when the input has more than one line equal to1, the output will be corresponding to the input with lowest subscript. For example if the inputs are I_3 =1 and I_1 =1 and the rest zero, the output should be 01.
Draw a truth table for this encoder and realize it using 2 input NOR gates. (5)

4. f is a function of A, B, C, D such that $f(A,B,C,D) = \prod(0, 1, 3, 4, 5, 7, 11, 13)$. Implement the function f using minimum number of 8-1 multiplexers and if needed, one additional gate. (2)

5. f_1 and f_2 are functions of A, B, C, D such that

$$f_1 = \prod(0, 3, 5, 11, 13)$$
$$f_2 = \sum(3, 7, 12, 13, 15)$$

Express $f_3 = f_1 \oplus f_2$ in a minimized Sum-of-Product form. (3)

6. Consider a 5-bit ripple carry adder. Each full-adder is implemented using a 3-input XOR gate, three 2-input AND gates, and one 3-input OR gate. Consider the delay of each 3-input XOR gate to be 4 nsec, the delay of each 2-input AND gate to be 2 nsec, and the delay of each 3-input OR gate to be 3 nsec. What will be the total time taken by the 5-bit ripple carry adder to perform a successful addition operation obtaining all the sums and carries? (3)