ECE 201 Digital Electronics Major Exam

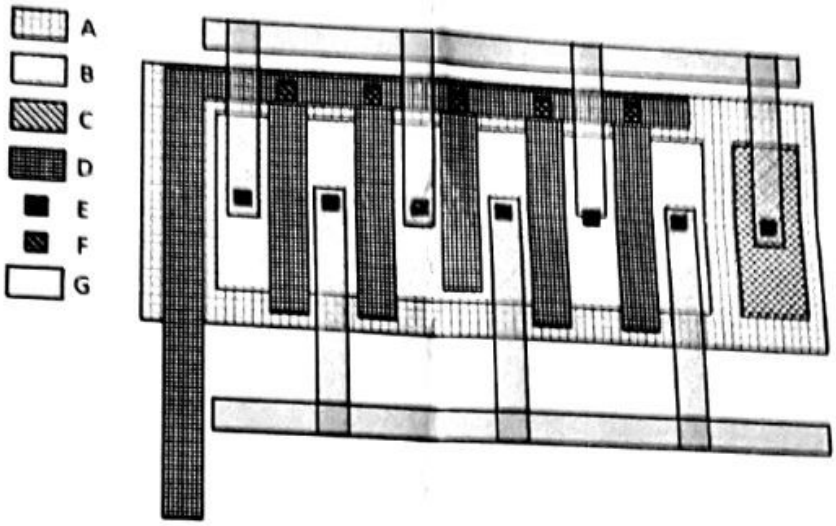
4th May 2018 **Max. Marks: 35**

This is a closed book exam. No books, notes or digital resources are permitted during the exam.

Important instructions

A. Please begin your **answer to each question on a new page**.
B. **All parts** of a question must be answered **together**.
C. Adoption of **unfair** means will lead to '**F**' grade in the course.

Q1. A CMOS technology based layout is shown. Assuming typical CMOS layer name assignments, what is the intended function of this device or circuit? Mention assumed layer name assignments to justify your answer. If you notice any issues in the layout, briefly mention them. **(6 marks)**



Q2. Implement the function F=[A.(B+C)+DE]' in dynamic logic at schematic level. **(4 marks)**

Q3. Make an FSM based data receiving and processing module. At the input, serial data comes in, separated by a frame separator 1101, i.e. sample data looks like **1101**XXXX**1101**XXXXXXX**1101**XX...

The machine has an output Y, which should be initialized to 0. Only if a continuous stream of at least three 1's or three 0's is detected in the input data, output should be raised to 1. Draw state diagram and state table. Perform state reduction if needed. Implement using D flip-flops. **(8 marks)**

Q4. Design a D-latch using asynchronous design principles. *(Please note that you are not to use the SR latch as a building block but derive the circuit using flow table. The specification is as follows.)*

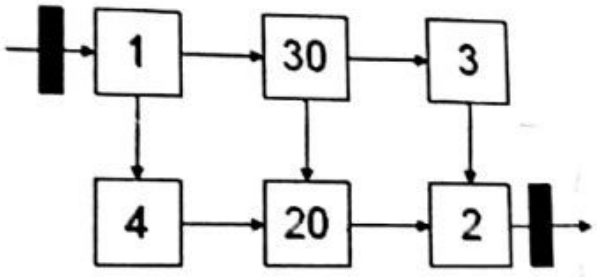
The latch has two inputs enable (g) and data (d), and one output (q). When enable is high, q follows d. When enable is low, output holds current state.

a) Draw the state transition table for this circuit, showing the stable states of the system

b) Derive a circuit for the above mentioned D-latch using NAND and NOT gates.

c) The setup time may be derived from fundamental mode restriction. When D, changes, the circuit takes some time to come to a stable state. The enable signal should not change during this time. Given the circuit, calculate the setup time, assuming NOT gates have delay of 0.25 ns, and NAND gates have a delay of 1 ns. **(8 marks)**

Q5 For the circuit below design a pipeline to maximize the throughput. What is the latency and throughput of your circuit? **(5 marks)**



Q6. Explain **(4 marks)**

1) Why,in 6T-SRAM design the PMOS transistor is inactive during memory read

2) How sense amplifiers make readout faster