ELL/EEL 201 Digital Electronics Minor2 Exam

24 March 2018 **Max. Marks: 20**

This is a closed book exam. No books, notes or digital resources are permitted during the exam.

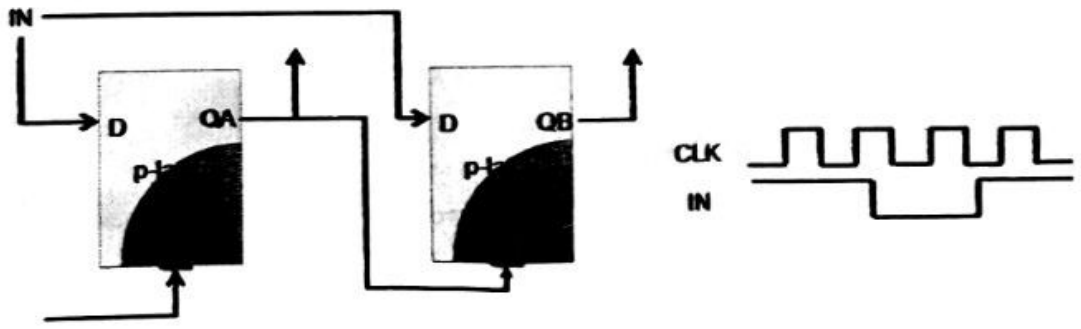
Important instructions

A. *Please begin your* ***answer to each question on a new page.***
B. ***All parts*** *of a question must be answered* ***together.***
C. *Adoption of* ***unfair*** *means will lead to* ***'F'*** *grade in the course.*

1. **(6 pts)** Serial data is coming on an input "X" and is being read left to right. Design a Moore FSM that detects presence of pattern {10110} on input "X" by raising output "Y" to a "1" ("Y" stays at "0" otherwise) each time the pattern is encountered, e.g. stream {1101011010} contains two valid patterns. Show (i) state diagram and (ii) state table for the Moore machine. Afterwards, convert this Moore machine to a Mealy machine using (iii) state table and finally show the (iv) state diagram of the Mealy machine. You may use state reduction as needed. Don't do any gate level implementation using flip-flops and combinational logic for this problem.

2. **(6 pts)** Desgn a 3-Bit Up/Down Gray counter using T-Flip Flops.

3. **(4pts)** Assume that the p-latches shown below have a small but finite setup time that is larger than their clk-to-Q/D-to-Q delay but less than half the period of CLK. There is no clock skew. Given the input signals CLK and IN, draw the timing diagrams (with respect to CLK and IN) of QA and QB.



4. **(4pts)** Anti-Lock Brakes: Design a FSM for an anti-lock brake system that accepts two inputs: WHEEL and TIME, and generates a single output -UNLOCK. The WHEEL input pulses high for one clock cycle each time the wheel rotates a small amount. The TIME input pulses high for one clock cycle every 10 ms. If the machine detects two TIME pulses since the last WHEELpulse, it concludes that the wheel is locked and UNLOCK is asserted for one clock cycle to "pump" the brakes. After UNLOCK goes high, the machine waits for two time pulses before resuming normal operation. Draw an ASM chart for implementing this machine and show an implementation using D Flip Flops