Total Marks: 45, Duration: 2 hr.

Major Test

Please Note:

1. **This is a closed book test; you are allowed only 3 sheets of paper with reference formulae and other text written on it.**
2. **Do not use any electronic devices during the test, except a non-programmable calculator.**
3. **Clearly write steps involved in subjective answers to facilitate partial marking.**
4. **Even if you have finished your test, DO NOT LEAVE your seat unless invigilators have collected and counted answer sheets or you have a medical emergency.**

Attempt all questions.

1. Starting with a 0.18-micron technology node, show idealized and constant voltage scaling of parameters to 0.13-micron technology node. You are supposed to make valid assumptions on 0.18 micron node starting parameters, such as gate length, supply voltage, gate-oxide thickness etc. Compare pre-scaled and scaled values of all the relevant parameters.

2. An NMOSFET device has target equivalent oxide thickness (EOT) of 0.8nm and work function of 4.56 eV. What will be the problems if this device is implemented using SiO2 and Poly-Si as gate dielectric and gate material respectively? If a high-k dielectric with dielectric constant (k)=1000 is used instead of SiO2, how will the device perform? Will there be an issue with parasitic capacitance due to this changed gate dielectric thickness? Explain and back your answers with relevant calculations.

3. You are asked to design a logic complementary metal-oxide-semiconductor (CMOS) technology. Specifications include supply voltage (V_{DD})=0.7V, intrinsic inverter delay of 1ps and static power dissipation of 70nW per invertor. Starting with translation of these circuit specifications to transistor design targets, do a thorough device design to achieve the circuit specifications. Clearly write all your assumptions, back your answers with calculations wherever possible. Assume wiring parasitics (R and C) to be negligible.

4. Draw a schematic and layout of a p-channel bulk Si MOSFET. Drawings should be complete (i.e. also show V_{DD} and ground lines/symbols, any voltage sources required in the schematic view) and clear enough to depict basic function of the device.

5. What is the origin of body/substrate-current (I_B) in bulk Si long-channel NFETs? Draw and explain how I_B behaves as a function of (V_{GS}-V_T) for various values of V_{DS}. Clearly draw the characteristics and explain trend in each part of the curve.

6. Qualitatively compare short-channel effects, saturation drain current, series resistance, and major fabrication steps between a bulk Si and fully depleted (FD) SOI-MOSFET. Your analysis should have sub-conclusion for each of these topics. Back your answers with illustrative figures wherever possible.

7. A junction diode is to be used as a solar cell, an image sensor, and light-emitting diode (LED). Discuss design of the diodes in terms of doping profiles and any other relevant aspects. Back your answers with calculations and band-diagrams or other figures wherever possible.

8. Discuss fabrication process for an NPN transistor and its operation in different regions. Why is NPN more popular than PNP transistor? Discuss pros and cons of BJT and CMOS technologies for digital-logic and high-speed applications.