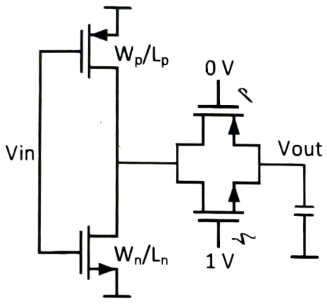
MOS VLSI DESIGN (ELL 734)

Major Examination

Instructions

1. Total duration is 2 hour i.e. from 8 am to 10 am.
2. Answer all questions. Maximum points is 30 points
3. If you feel any missing information in questions, Please assume variables and solve it
4. Use of class lecture or lecture notes or google search or text book is not permitted
5. State your assumptions clearly and write all intermediate steps.

1. Calculate the Logical effort of the circuit? Wp =2Wn (2 pt)



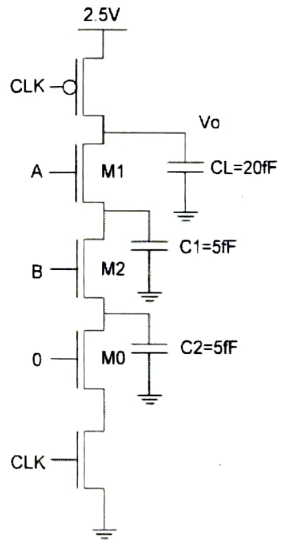
2.

a) Assuming that all the inputs of the circuit are initially 0 during precharge phase and that all internal nodes are at 0, Calculate voltage drop on V_o if A changes to 1 (Vdd =2.5V) during the evaluation phase. V_{t0} =0.5V. $2f_F$ =0.6V and ¥ =0.4 $V^{0.5}$. Include body effect (3 pt)

($V_T = V_{T0} + ¥(sqrt(2f_F + V_{SB}) - sqrt(2f_F))$).

b) Calculate Voltage drop on V_o if both A and B change to 1 (under above conditions) (3pt)

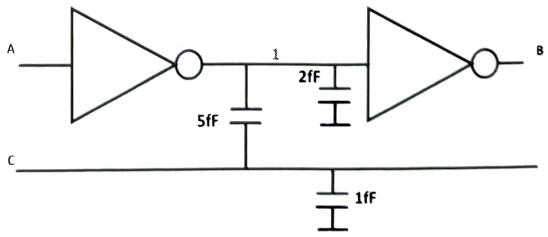
c) What is the maximum number of transistors that can be connected in series to M1 and M2 (including M1 and M2, excluding M0) of the output should not fall below 0.9V during the evaluation phase? Assume that each one of the new transistors has the same intrinsic capacitance to ground as M1 and M2 (C=5fF) (2pt)



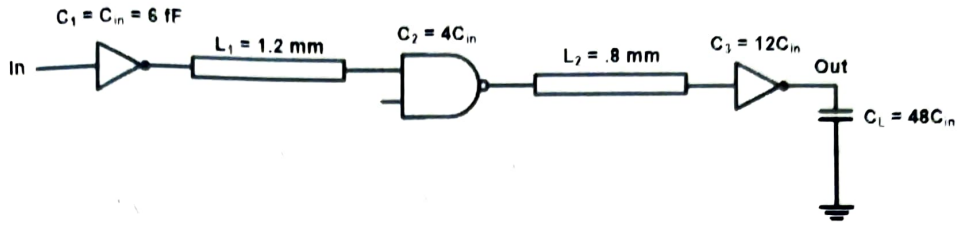
3. There are two inverters in the circuit. Signal C travels parallel to the routing of the inverters. Assume power supply to be 1V? (5pt)

a) For the best delay what should be transitions at A and C (2pt)

b) What should be noise margin of the inverters for the proper functioning of the circuit? (3pt)



4. R_W = 0.075 ohms/sq, W=0.2um, C_w = 0.2fF/um (this number includes the effects of both parallel plate and fringe capacitance). For the gates assume Vdd=1.2V and for transistors assume C_g =2fF/um, C_d =1.6fF/um, Rnmos =10k/sq and Rpmos = 20k/sq. Assume transistor are long channel devices. Gate sizes are shown below where Cin =6fF (5pt)

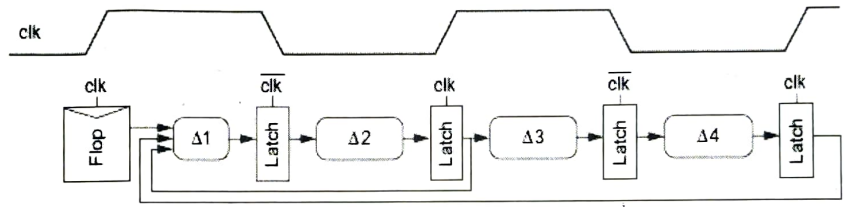


a) Draw an RC model for the above circuit and express the delay from In to Out in terms of L_1, L_2, and transistor and wire parameter. Use pi model for the wire.

b) Using the expression from part (a), find the total delay of the chain?

c) Now, lets reorganize this chain in order to reduce the delay. Assume that the total length of the wires is constant (L_1 +L_2 =2um), what values of L_1 and L_2 give us the optimal delay for the chain? Assume that the size and order of the gates are fixed, and that this path remains critical regardless of how L_1, L_2 change. Using these optimal values of L_1, L_2, what is the optimal delay of the chain under these conditions?

5. Determine the minimum clock period at which the circuit below will operate correctly for each of the logic delays. Assume there is zero clock skew and the latch delays are accounted for in propagation delay. (5pt)

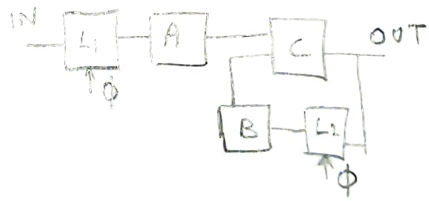


a) Δ_1 =300ps, Δ_2=400ps, Δ_3=200ps, Δ_4=350ps

b) Δ_1 =300ps, Δ_2=400ps, Δ_3=400ps, Δ_4=550ps

c) Repeat a and b for clock skew of 100ps.

6. Consider the simple state machine shown above, A,B and C represent combinational logic blocks with the following properties (5 pt)



$T_{logic,mina}$ = 200ps, $T_{logic,maxA}$ = 1ns.

$T_{logic,minB}$ = 300ps, $T_{logic,maxB}$ = 2ns.

$T_{logic,minC}$ = 100ps, $T_{logic,maxC}$ = 0.5ns.

The L-units represent positive latches clocked with (phi). These latches have a setup time of 150ps and t_{d-q} of 250ps. The clock to output delay t_{c-q} is 100ps and t_{hold} is 100ps. The clock has a period Tclk and is high for a duration of Ton (Duty cycle is Ton/Tclk)

a) Determine the conditions on the clock necessary to avoid the occurance of hold time violations?

b) Determine the absolute minimum clock period for this circuit to work correctly as well as the maximum duty cycle