Electrical Engineering Department

ELL734 MOS VLSI Minor I Time: 1hour; Marks: 20

Q1. Realize $Z = \overline{(A+B)C+D}$ using single stage static CMOS gate. Signal C arrives last.

Size the NMOS and PMOS transistors.

The output Z is the input to 3 reference inverters. Find the propagation delay using Logical Effort Method. Assume t_{p0} is known.

[4+3+5=12]

Q2. (a) Plot the Voltage Transfer Characteristics (VTC) of a 2 input NOR gate. Also plot VTC of reference inverter on the same plot.

(b) Calculate the dynamic power dissipation at the output node of the 2 input NOR gate.

[5+3=8]