MOS VLSI DESIGN (ELL 734)

Minor Examination

**Instructions**

1. Total duration is 1 hour i.e. from 8 am to 9 am.
2. Answer all questions. Maximum points is 25 points
3. If you feel any missing information in questions, Please assume variables and solve it
4. Use of class lecture or lecture notes or google search or text book is not permitted
5. State your assumptions clearly and write all intermediate steps.

1. Assume that in the technology the PMOS mobility is **thrice** lower than the NMOS mobility.

- What is the logic realized? (2 pt.)
- Size the PMOS and NMOS transistors for equalizing the rise and fall time as of unit Inverter? (7 pt.)
- Compute the worst case Elmore delay for the rising and falling edge? (5 pt.)

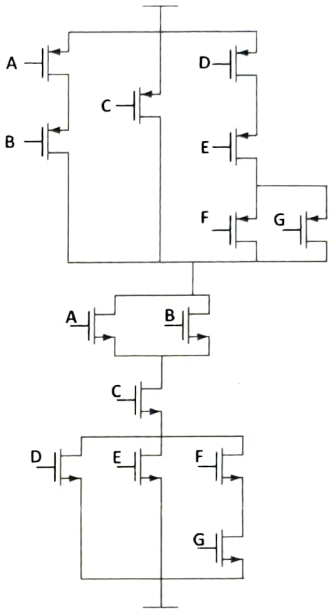


**Figure 1**

2. Plot the VTC of the circuit in Fig 2 and identify the operating region of transistors? (5 pt.)

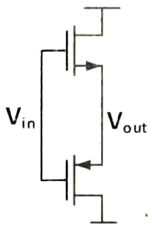


**Figure 2**

3. Compute X, Y and Z for the circuit shown below? (6 pt.)